ATLAS MDT Trigger Processor Demonstrator

Digital Board for Fast Procession of a Huge Amount of Data in Real Time

Motivation

- High raw data rate from the muon subsystem of the ATLAS detector of ≈ 10 Tb/s cannot be stored for offline analysis.

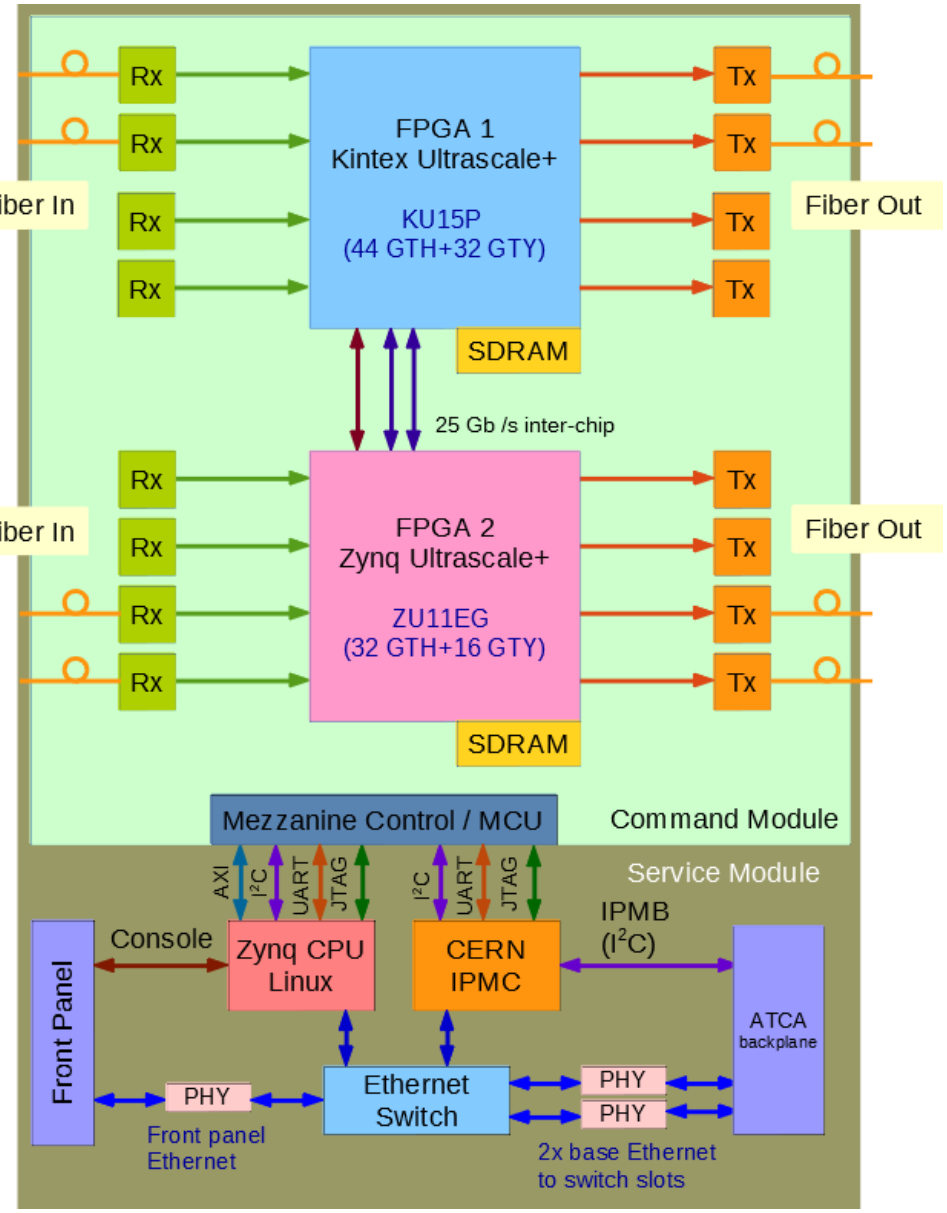
$\Rightarrow$ Perform a quick analysis of the incoming data to discarding data that is not interesting.

$\Rightarrow$ Build a dataset of potential interesting events.

Technical Realization

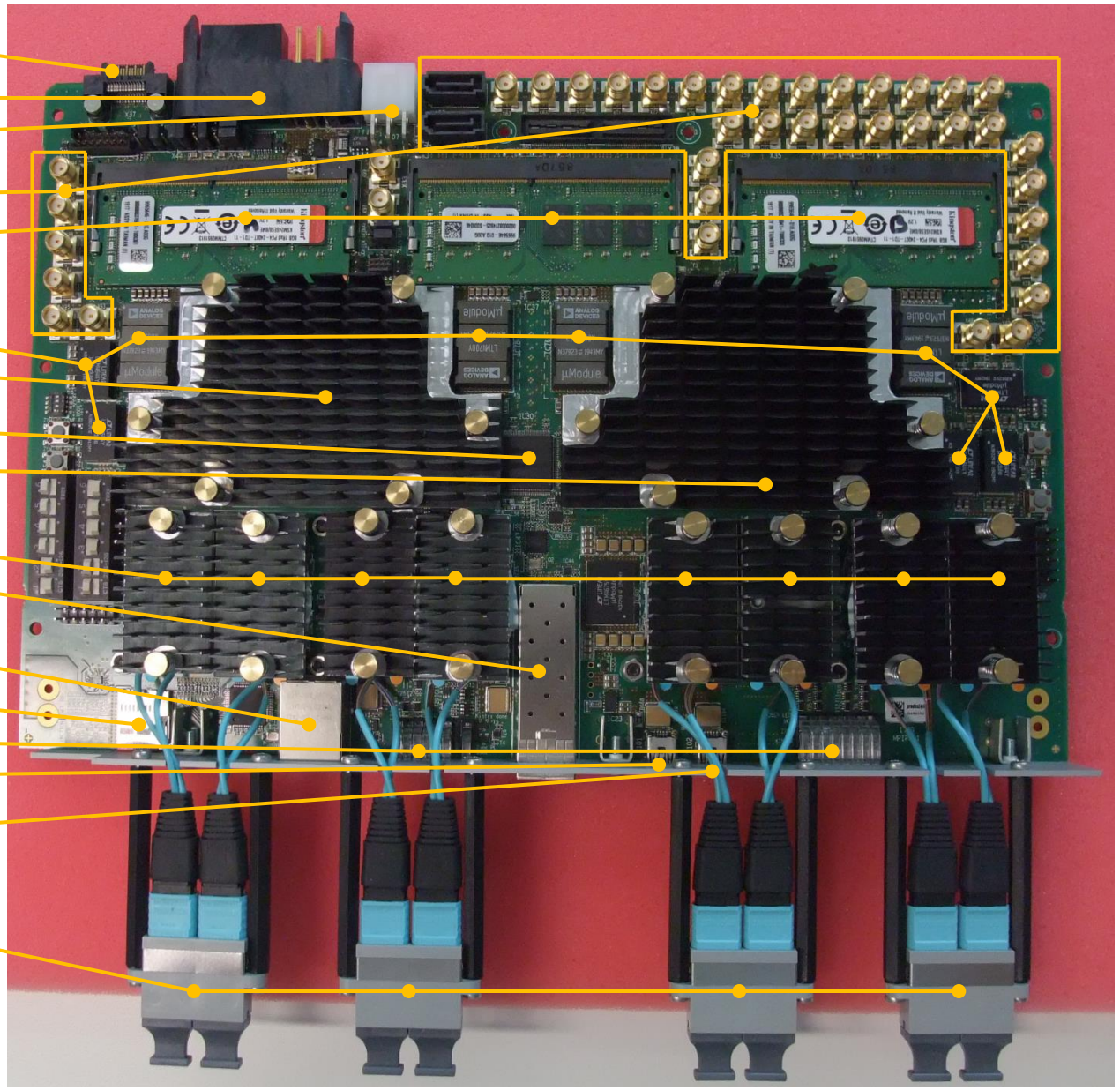
- Set of 64 high-performance computing blade.
- Each blade has 192 fibers with a total raw bandwidth of 3.5 Tb/s.
- Powerful data processor running a dedicated low-latency algorithm in real time.
- Perform a quick analysis of the incoming data to discarding data that is not interesting.

Block diagram

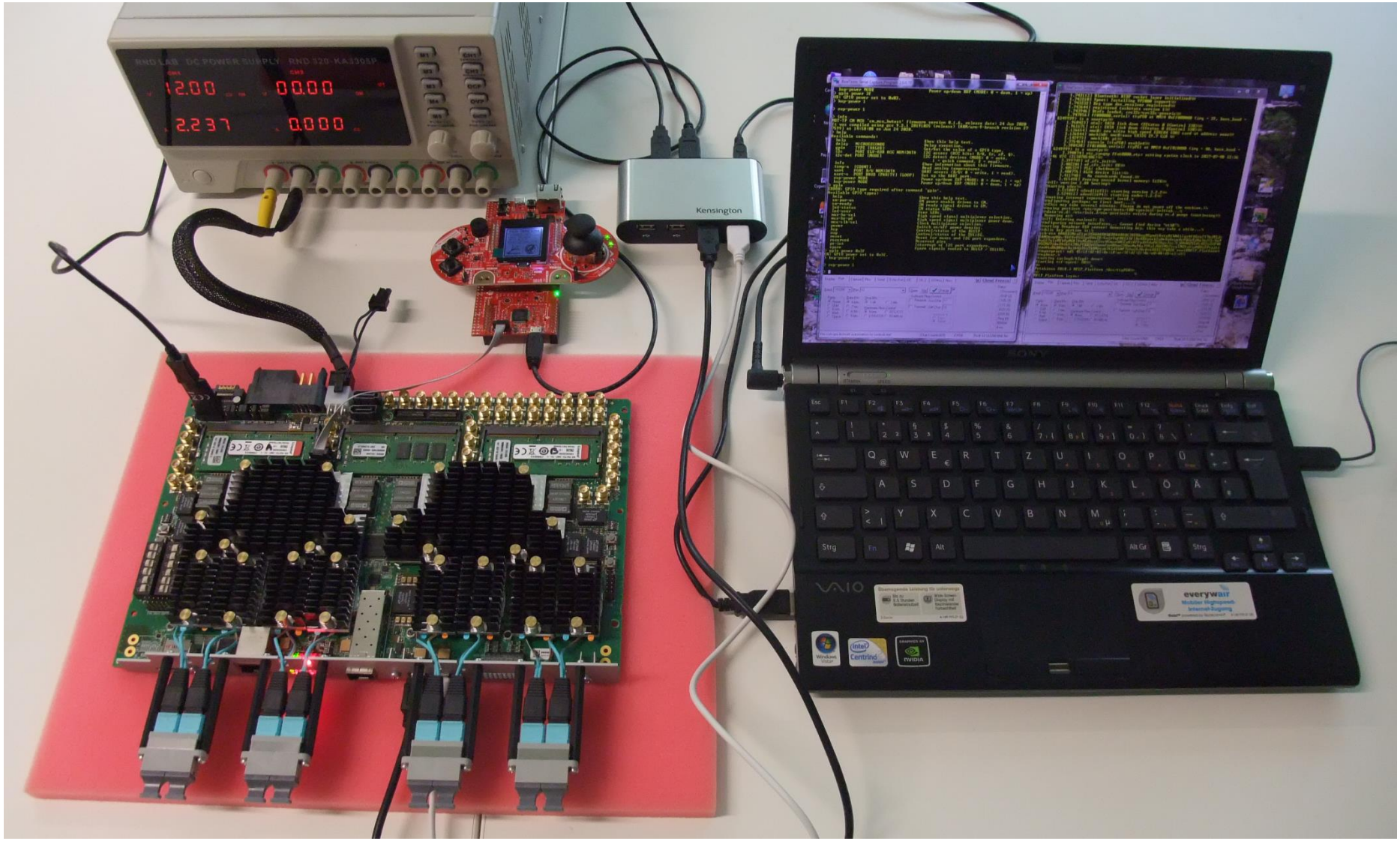


- Standard ATCA blade called “Apollo”.
- Alluding the NASA Apollo 11 mission, it consists of a Service Module (SM) and a Command Module (CM).
- Service Module:
  - Interface to ATCA infrastructure.
  - Slow control (DCS) path.
  - +12 V power.
- Command Module:
  - Optical interfaces (FireFlys):
    120 fibers @ 14 Gbps,
    72 fibers @ 25 Gbps:
    - Front-end (FE)
    - Sector logic (SL)
    - DAQ + TTC (FELIX)
    - Neighbors
  - Large Xilinx UltraScale+ FPGAs including option for ARM cores
  - MCU for control and monitoring

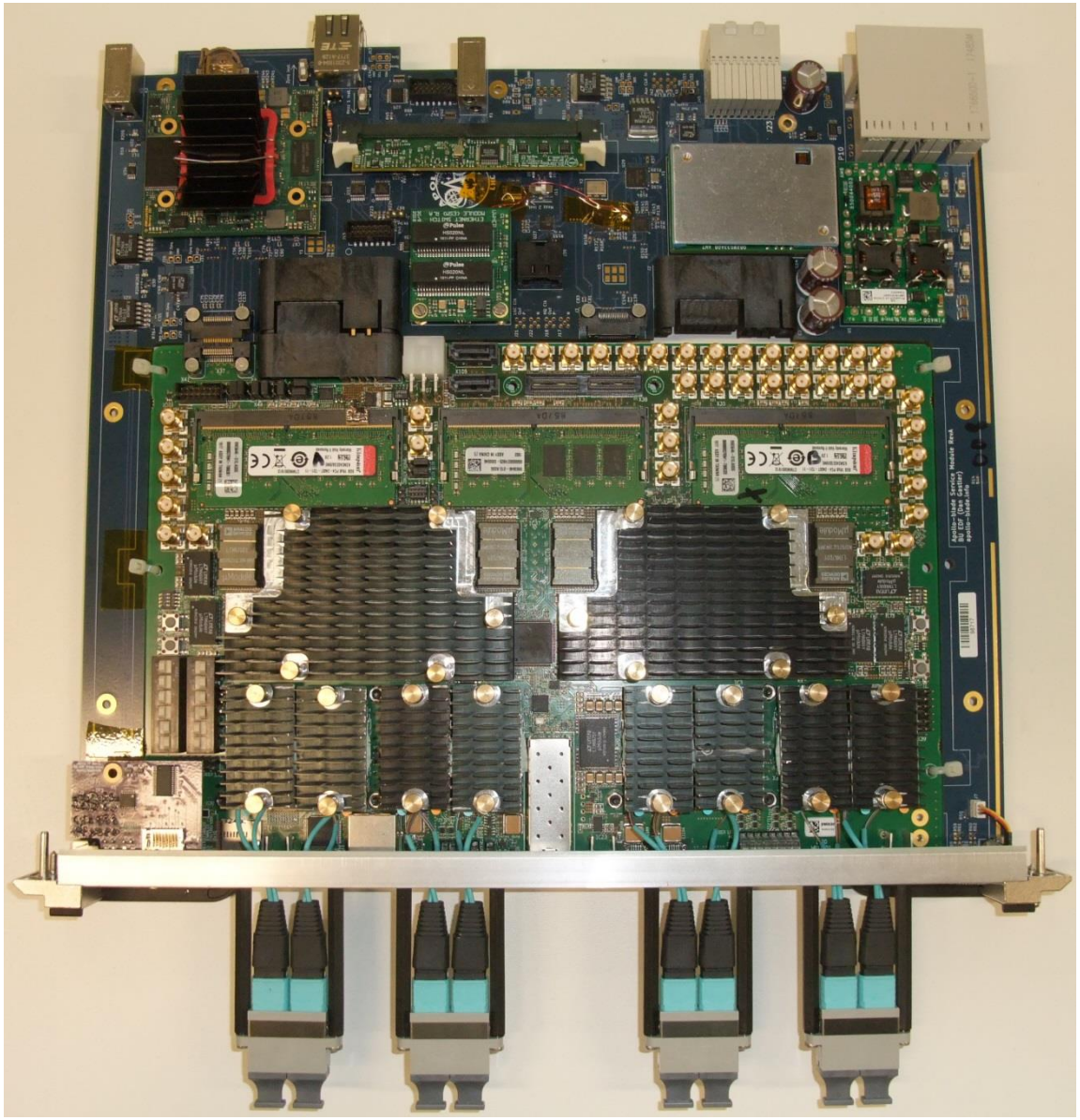
The “Brain” of the System



Test Setup in the Lab



Complete Module + 19 “ Shelf



One shelf can host up to 14 modules.