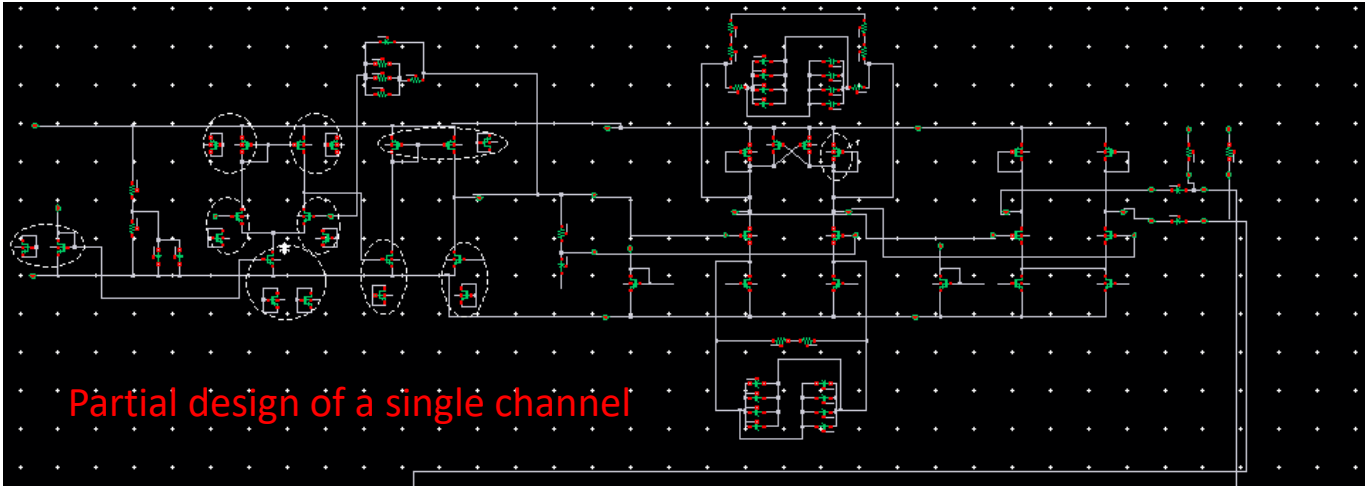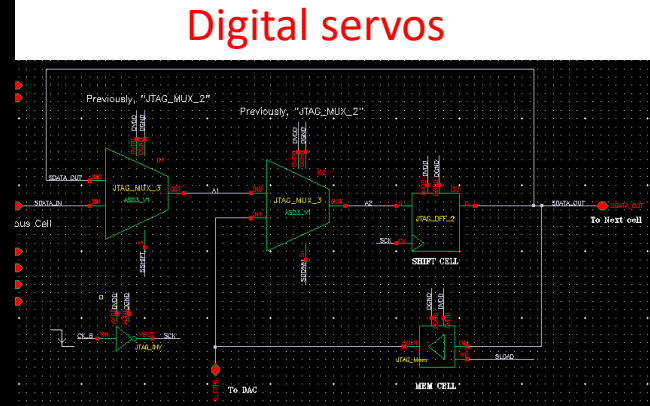# ATLAS MDT ASIC (Example)
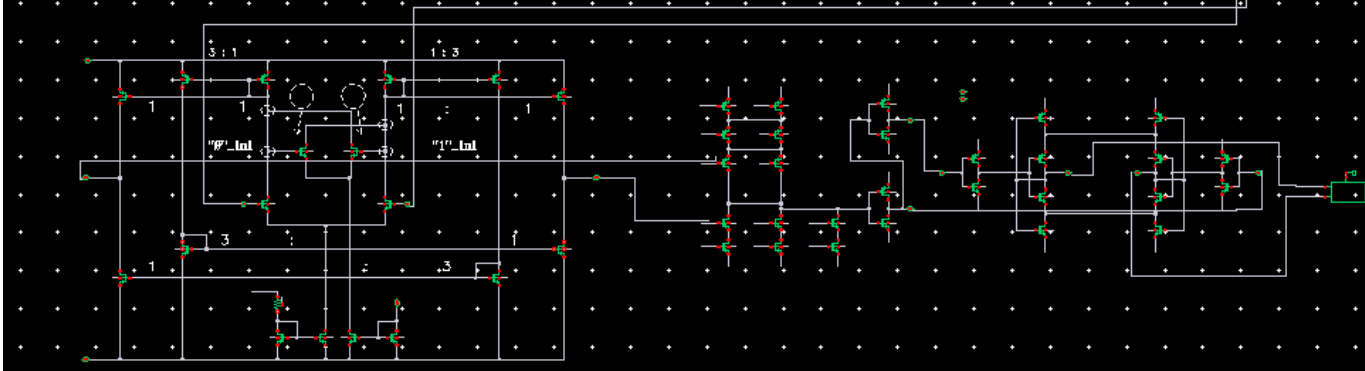
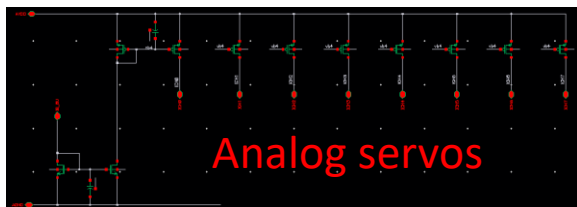⌘ A part of the schematic design for the new MDT ASIC:

Digital servos

Partial design of a single channel
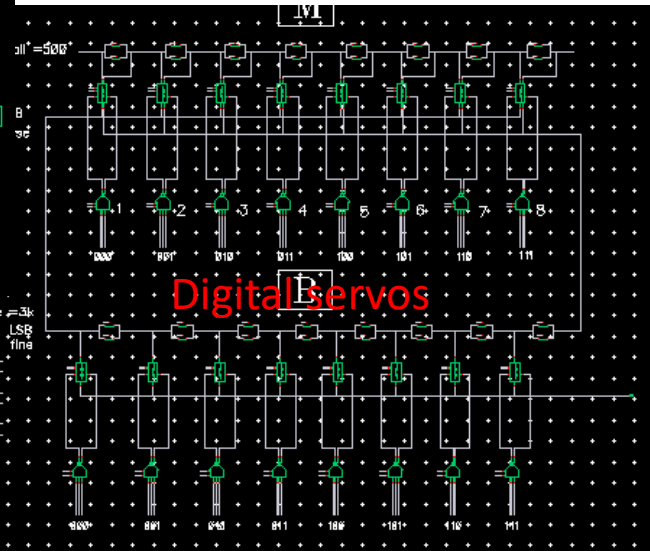
Analog servos

Analog servos
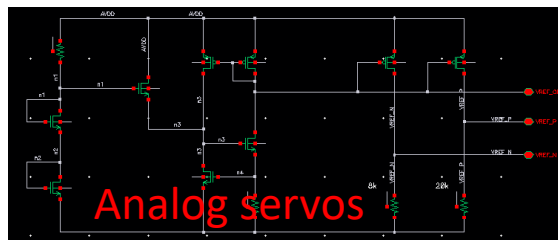
Digital servos

ATLAS MDT ASIC (Example)

⌘ An example of layout design for a **small** analog block

Decoupling-Cap For Dummy Differential Output node

Amplifier Core

Decoupling-Cap For Dummy Differential Input node
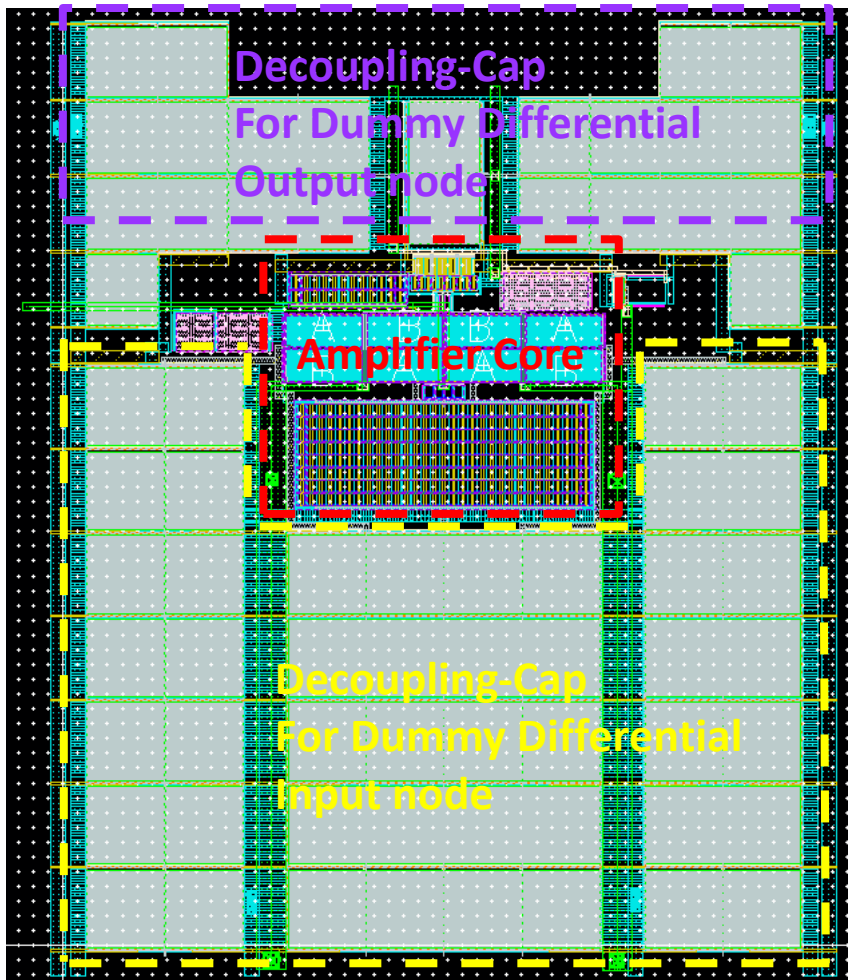
No.	Layout Net	Source Net	C Total (F)	CC Total (F)	C+CC Total ...
1	AGND	AGND	1.07543E-12	9.32384E-11	9.43139E-11
2	preamp_ib	PREAMP_IB	3.05180E-13	6.66730E-11	6.69782E-11
3	preamp_ob1	PREAMP_OB1	1.09213E-13	2.68407E-11	2.69499E-11
4	AVDD	AVDD	5.80906E-12	1.26429E-11	1.84519E-11
5	X86/40	XI0/A	5.41894E-14	9.96119E-13	1.05031E-12
6	preamp_ia	PREAMP_IA	5.83134E-14	6.35100E-13	6.93414E-13
7	IBIASPREAMP	IBIASPREAMP	6.52206E-14	3.77046E-13	4.42267E-13
8	X86/41	XI0/NET_016	7.41815E-15	4.22880E-13	4.30298E-13
9	X86/42	XI0/NET038	7.11473E-15	4.17066E-13	4.24180E-13
10	preamp_oa1	PREAMP_OA1	2.09393E-14	7.06264E-14	9.15657E-14
11	X86/43	XI0/NET_019	4.35816E-15	2.46339E-14	2.89921E-14
12	48	VSF	8.65954E-16	2.89562E-16	1.18561E-15
13	7		2.35543E-16	8.38137E-17	3.19357E-16
14	9		2.35543E-16	8.25752E-17	3.18118E-16
15	11		2.35543E-16	8.01512E-17	3.15694E-16
16	5		2.46888E-16	6.45995E-17	3.11488E-16
17	23		2.35543E-16	7.27709E-17	3.08314E-16

☒ Find Nets: [   ] 🔍▾   Coupling to: ◆ All Nets ○ Specified Nets [   ] 🔍

⚙ preamp_oa1 ✕

Type	Count	
▣ C ▣	1	
⊟ cc CC ▣	10	
└ cc 6	1	
└ cc 40	1	
└ cc AGND	1	
└ cc AVDD	1	
└ cc IBIASPREAMP	1	
└ cc preamp_ia	1	
└ cc preamp_ob1	1	
└ cc X86/41	1	
└ cc X86/42	1	
└ cc X86/43	1	

Layout Net: preamp_oa1   Source Net: PREAMP_OA1   Coupled Capacitors: CC

No.	To Layout Net	Value (F)	To Source Net
1	preamp_ia	3.95551E-14	PREAMP_IA
2	IBIASPREAMP	1.56265E-14	IBIASPREAMP
3	X86/43	6.08275E-15	XI0/NET_019
4	AVDD	5.11911E-15	AVDD
5	preamp_ob1	3.06999E-15	PREAMP_OB1
6	AGND	7.99906E-16	AGND
7	X86/42	2.42566E-16	XI0/NET038
8	X86/41	7.58440E-17	XI0/NET_016
9	40	3.22896E-17	VSF
10	6	2.23825E-17	

An example of the extraction list for post-layout verification and validation